Towards Beneficial Hardware Acceleration in HAVEN: Evaluation of Testbed Architectures

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Motivation

- Verification of HW

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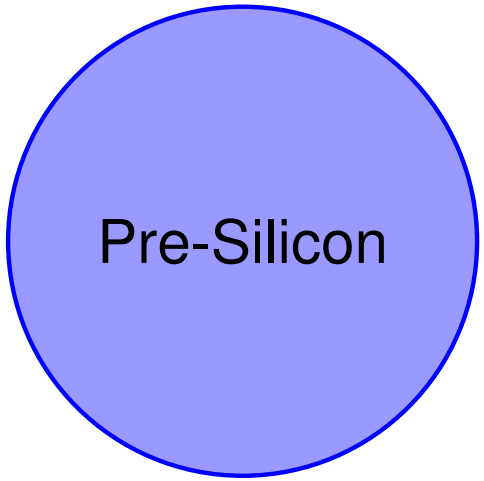

  - simulation & testing
  - formal verification
  - functional verification

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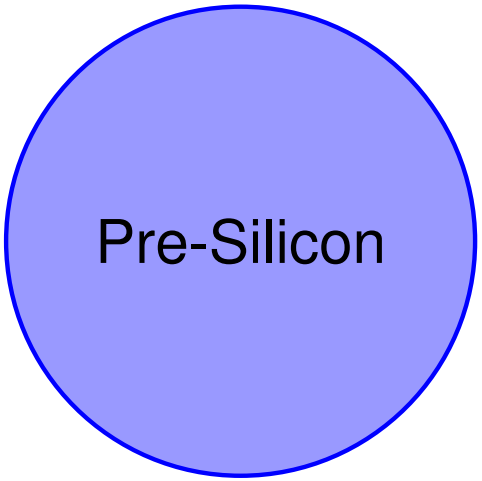

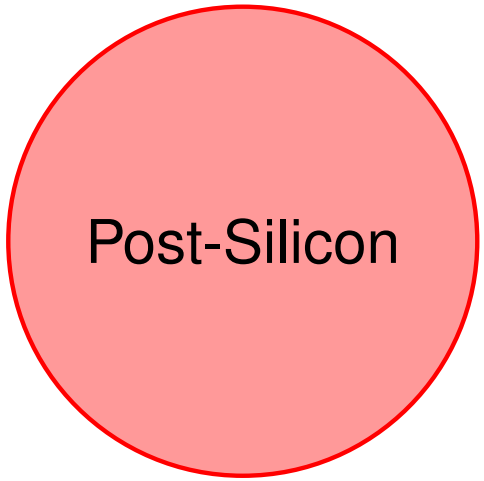

- simulation & testing
- formal verification
- functional verification

- prototypes

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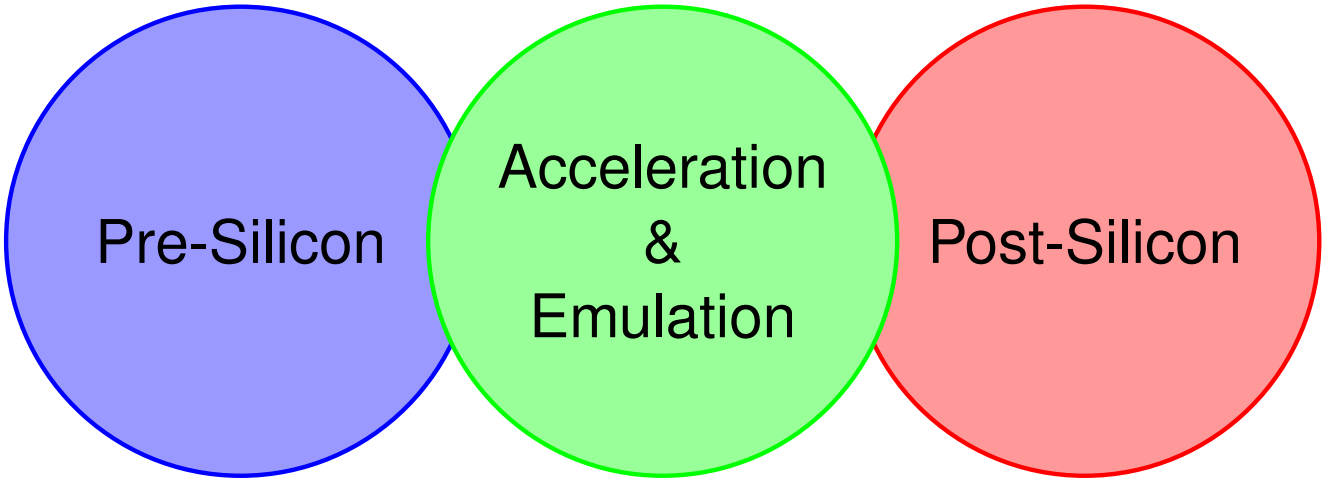

HAVEN

Functional Verification

Testbenches in SystemVerilog:

Functional Verification

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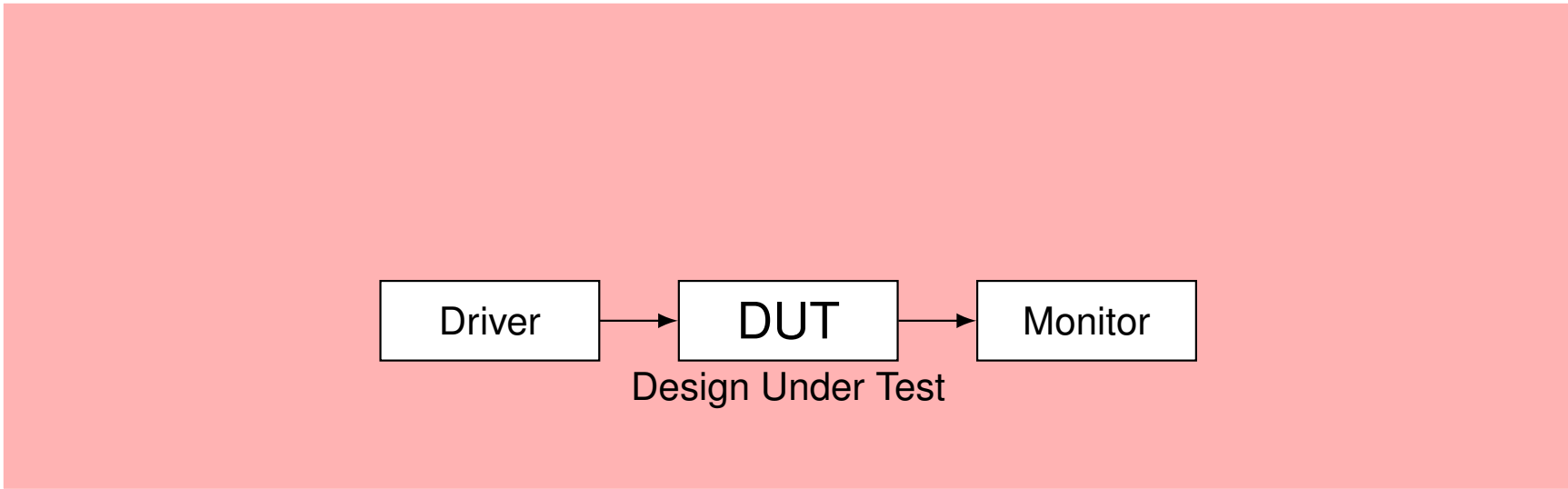
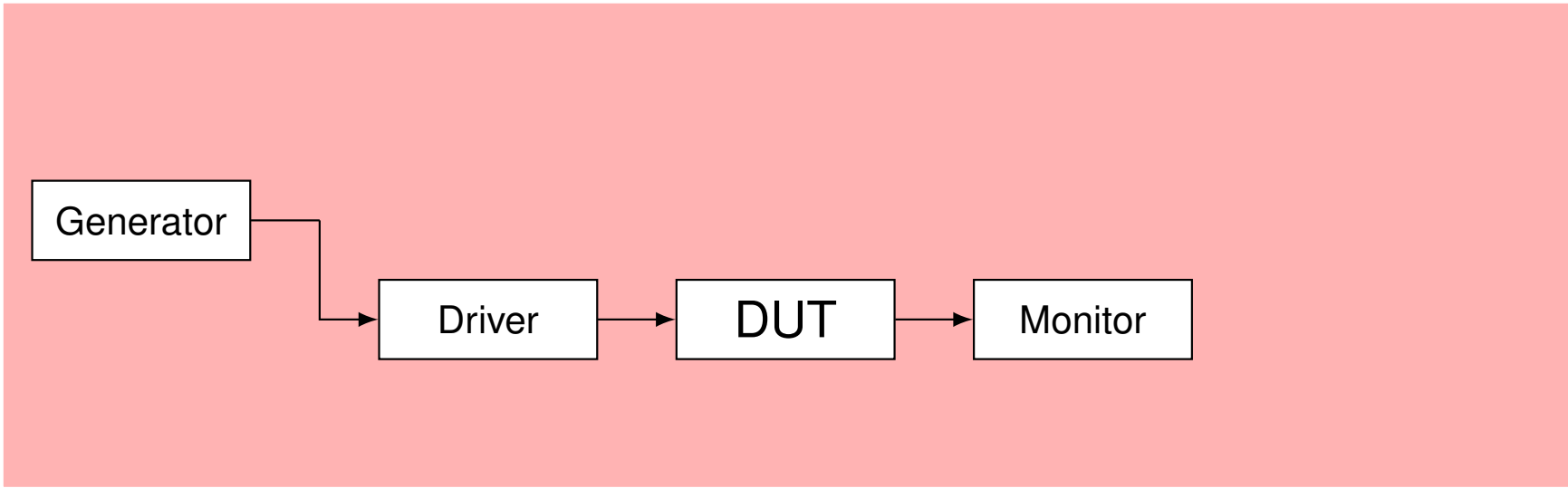


Functional Verification

Testbenches in SystemVerilog:

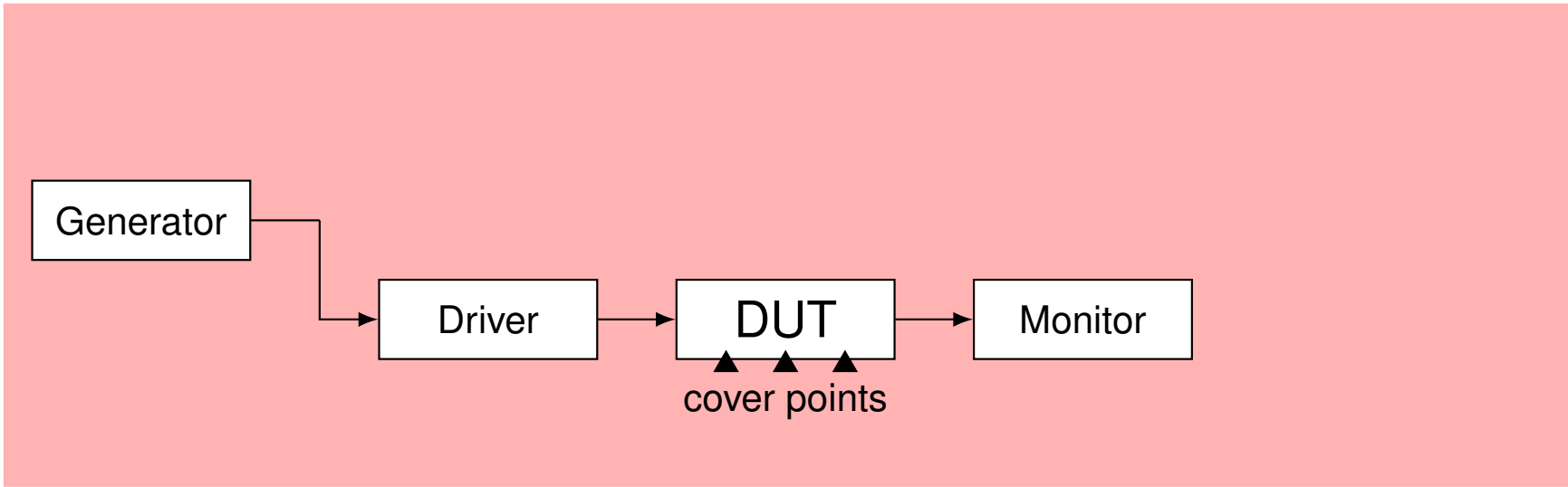
- constrained-random test vectors



Functional Verification

Testbenches in SystemVerilog:

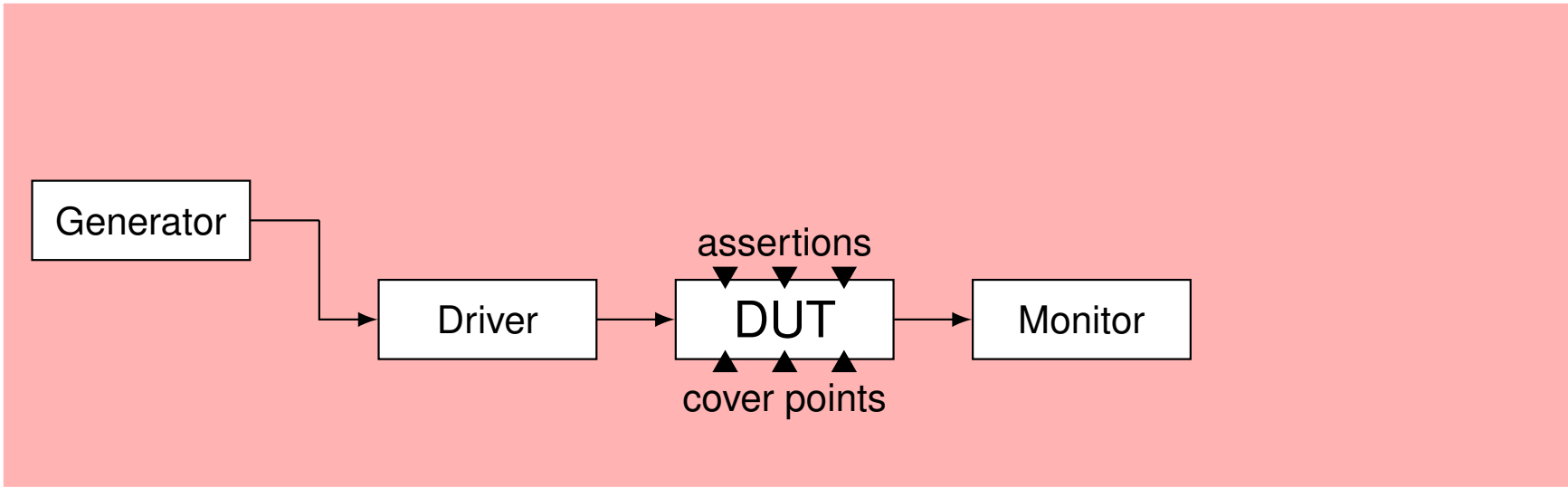
- constrained-random test vectors
- coverage



Functional Verification

Testbenches in SystemVerilog:

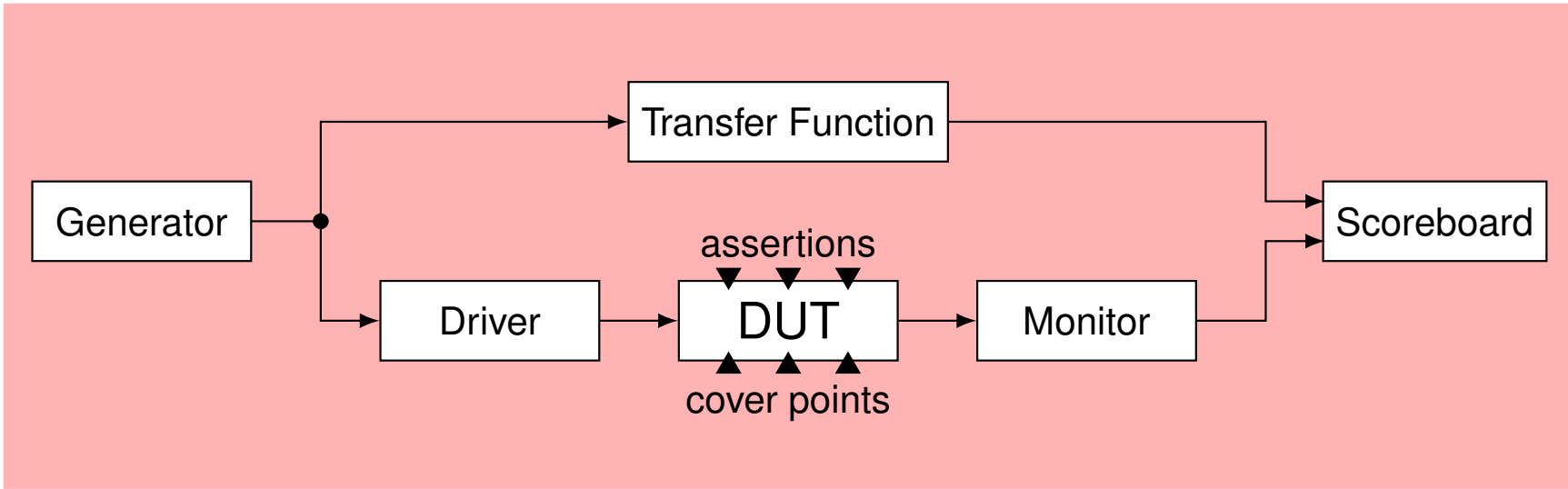
- constrained-random test vectors
- coverage
- assertions



Functional Verification

Testbenches in SystemVerilog:

- constrained-random test vectors
- coverage
- assertions
- self-checking



Acceleration

- Emulators
  - Mentor Graphics' Veloce, Cadence's TBA, ...
  - ☺ observability, assertions, coverage
  - ☹
    - proprietary & expensive $$$,
    - limited frequency (1–2 MHz).

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  - VHDL/Verilog ☺
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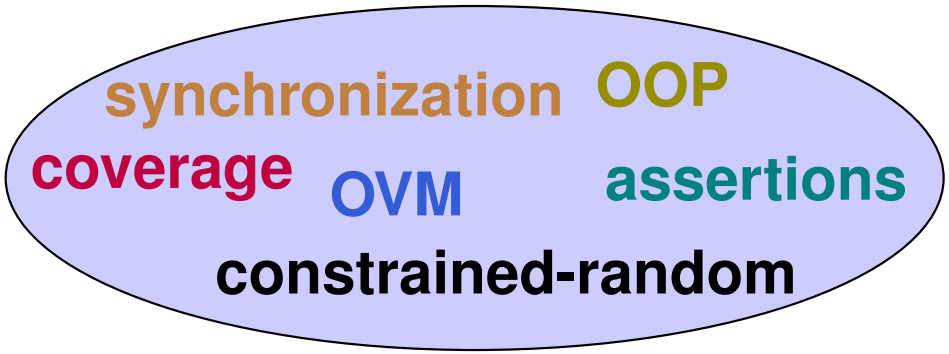
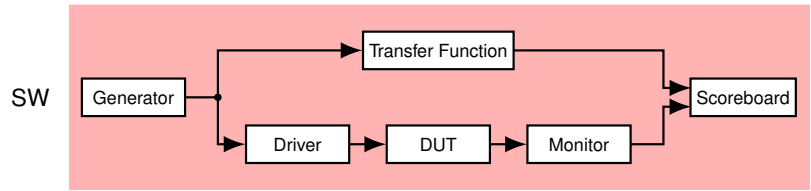


HAVEN

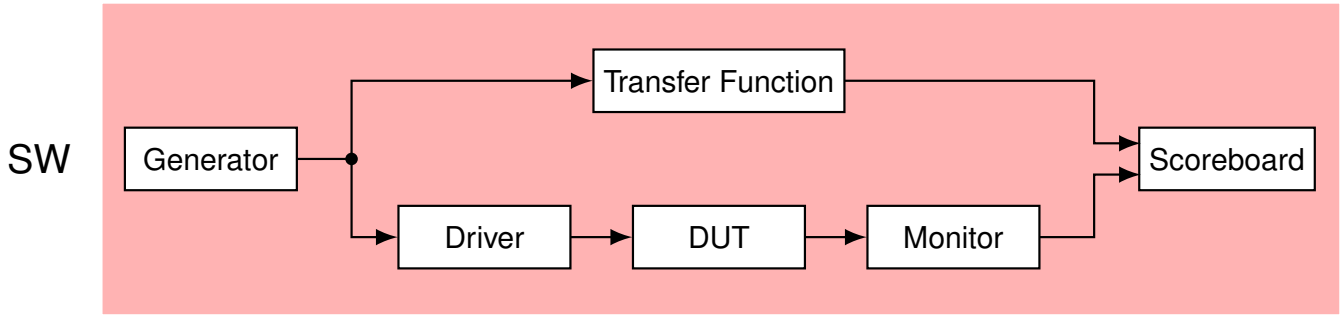
- move blocks into FPGA
  - Xilinx Virtex-5
- extendable/adaptable
- cycle-accurate
- synchronous units



HAVEN Testbed Architectures

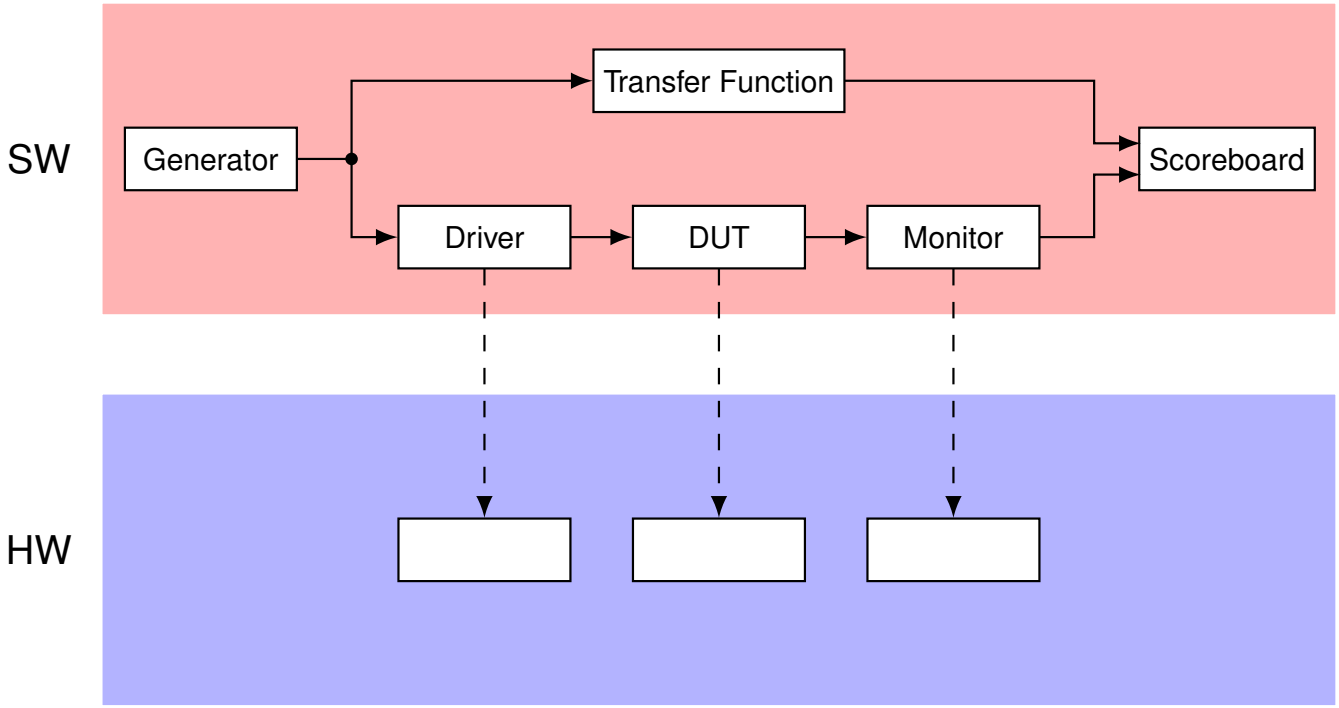
- 5 testbed architectures
- step-by-step acceleration
- trade-off: acceleration vs. observability

SW-FULL

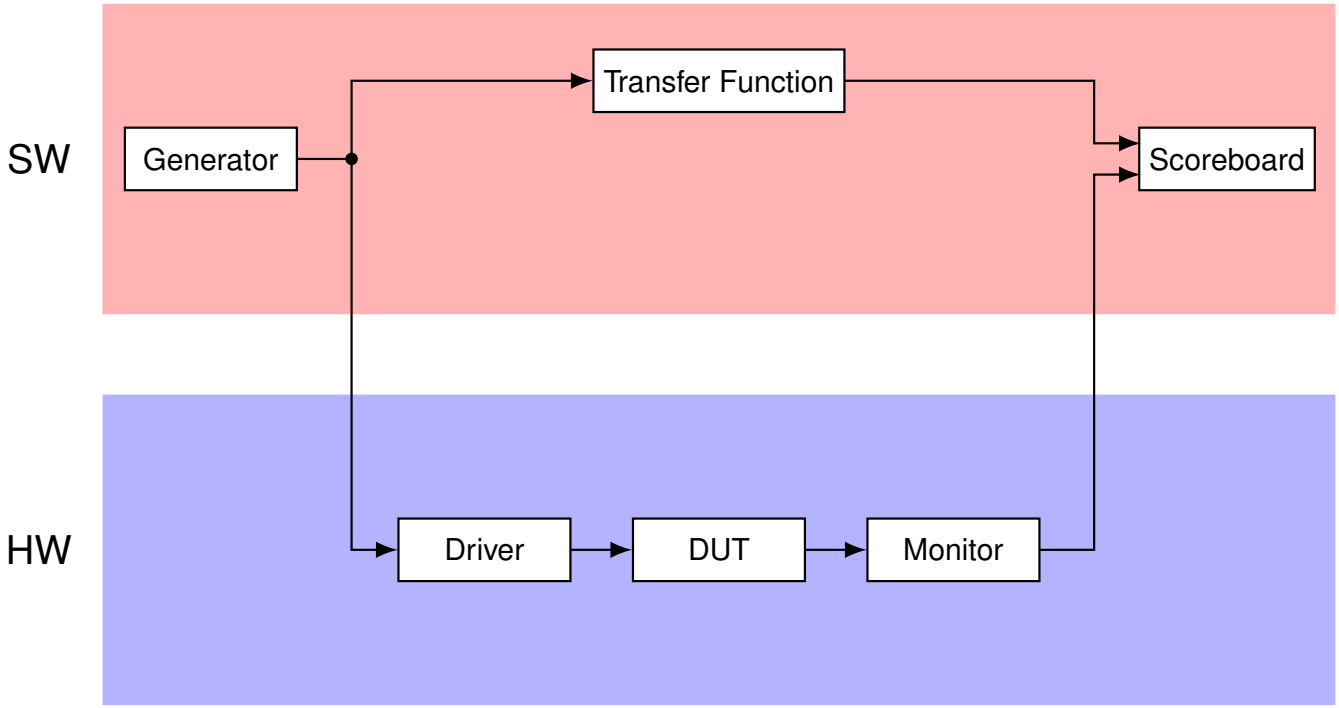


- ☺ observability
- ☹ performance

HW-DUT

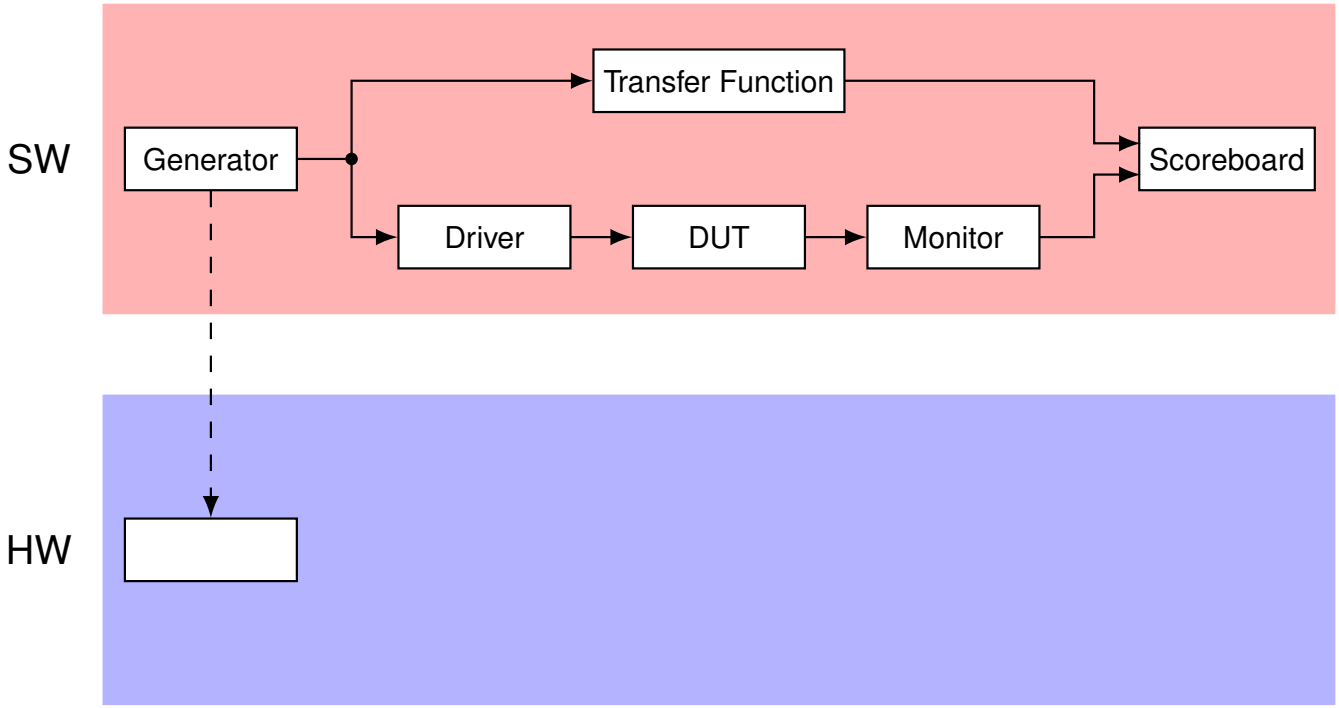

SW
HW
Generator
Transfer Function
Scoreboard
Driver
DUT
Monitor

HW-DUT



- observability
- assertions
- coverage

HW-GEN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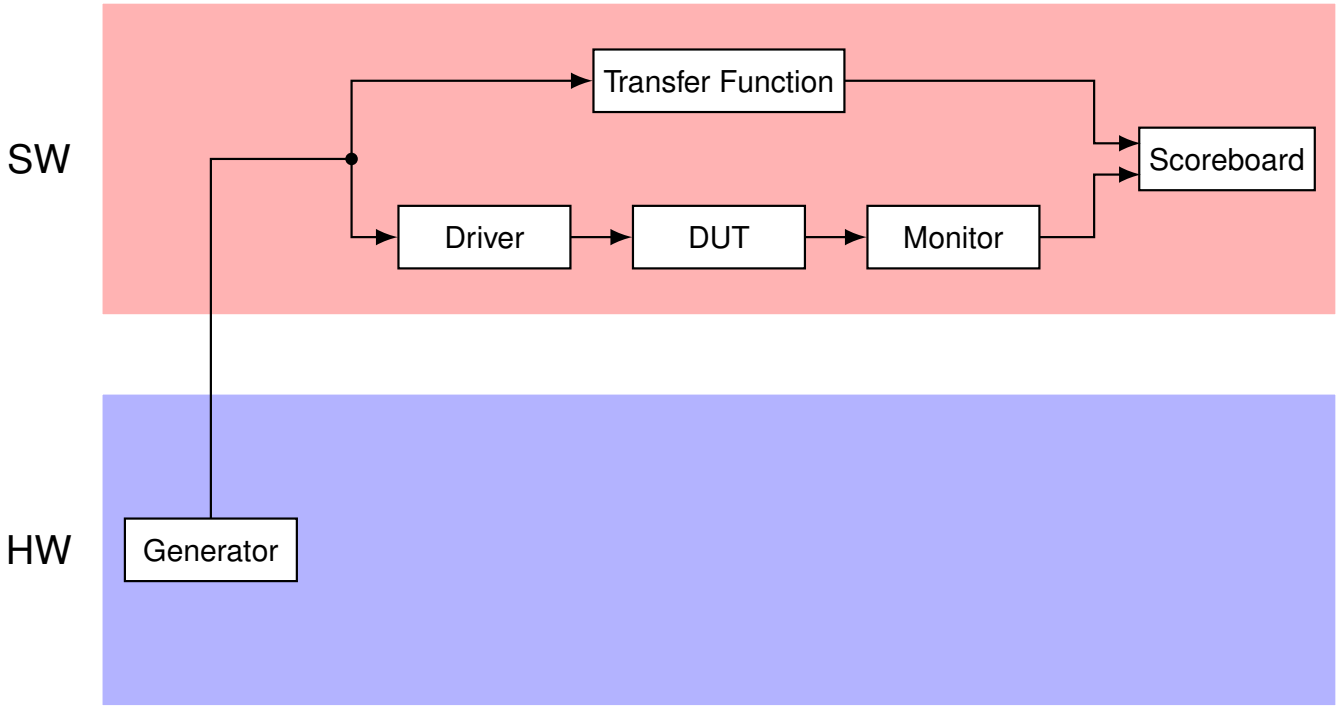
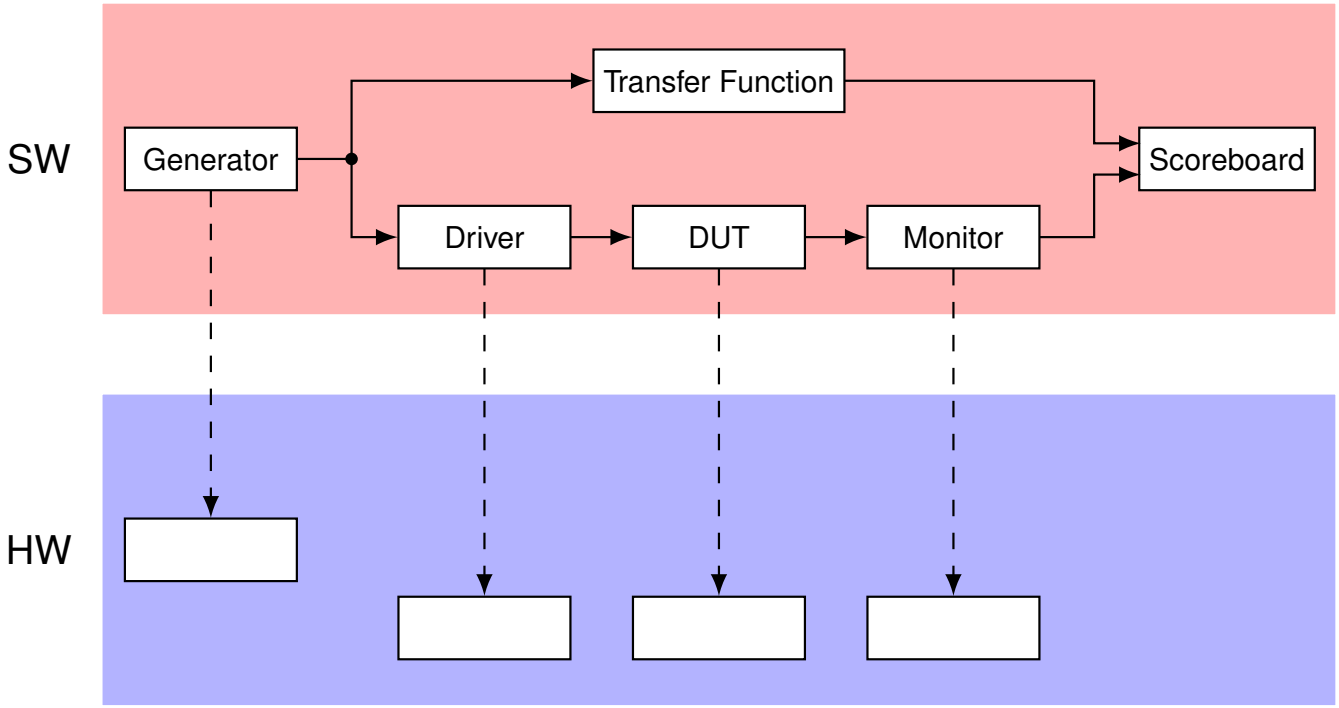


- HW Mersenne Twister
  - configurable from SW

HW-GEN-DUT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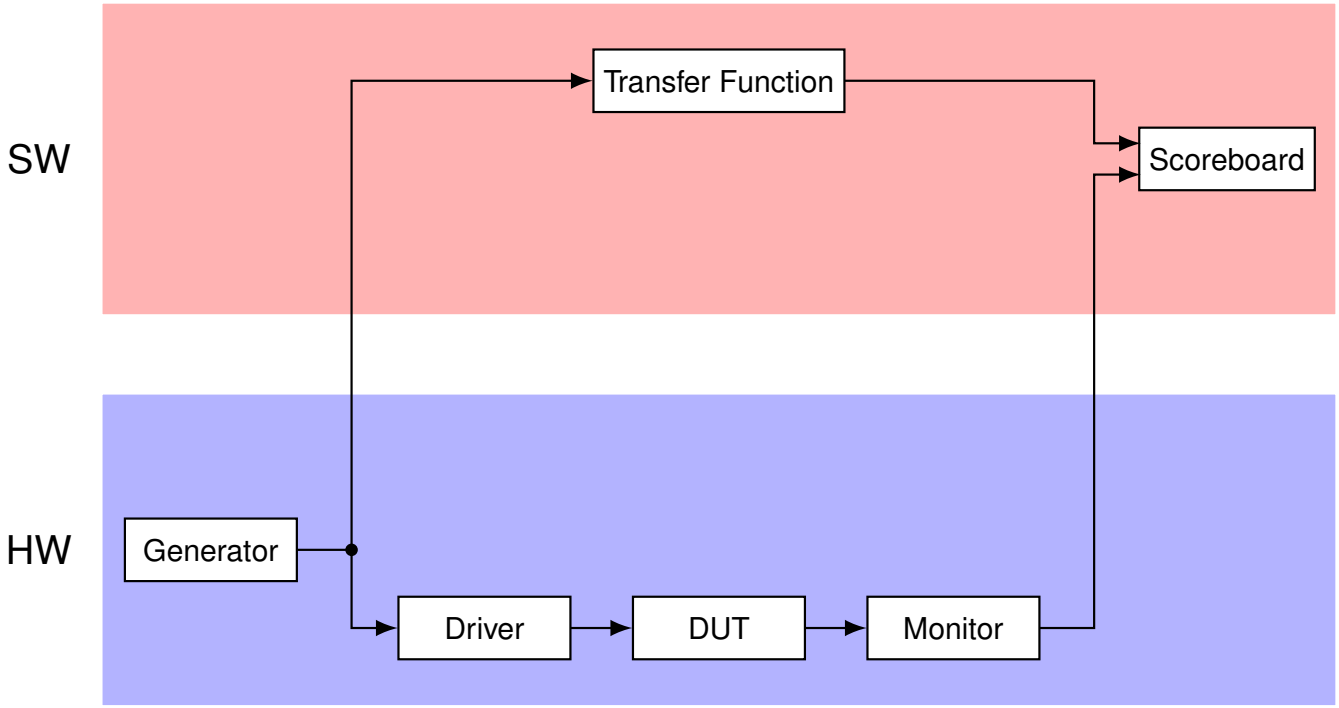
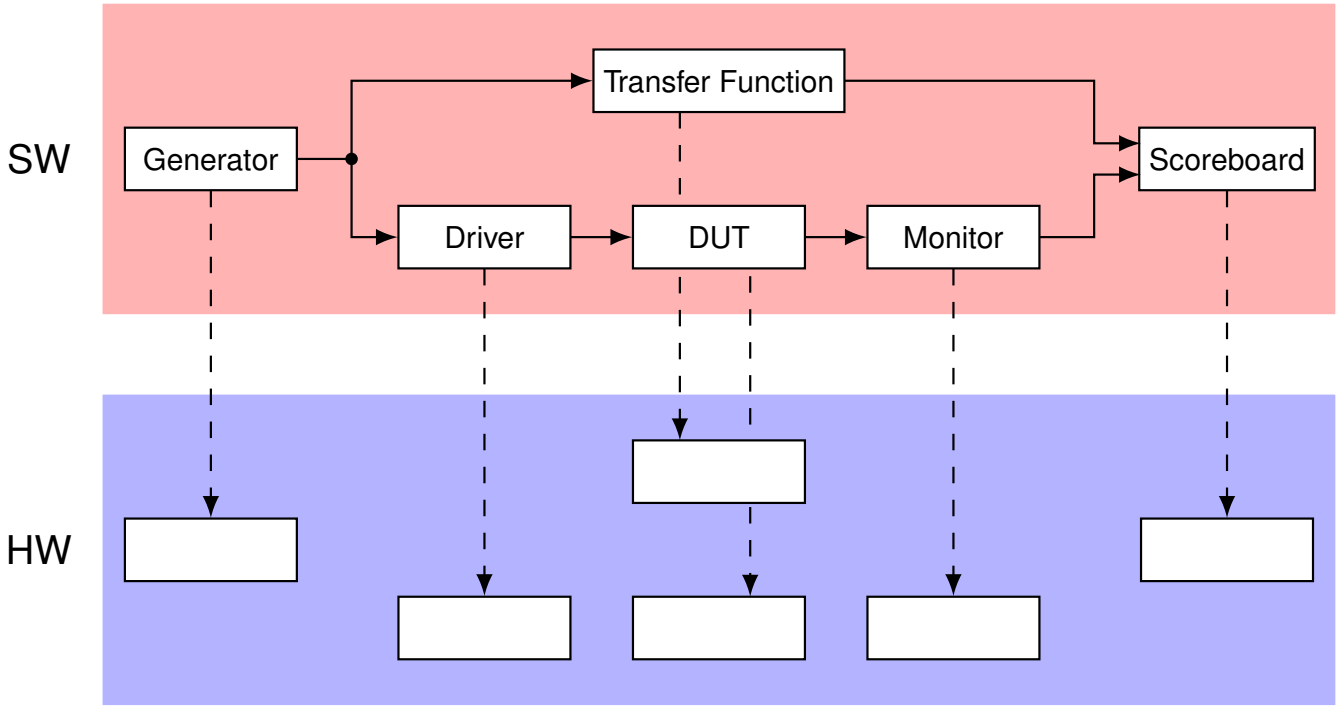


- existing transfer function

HW-FULL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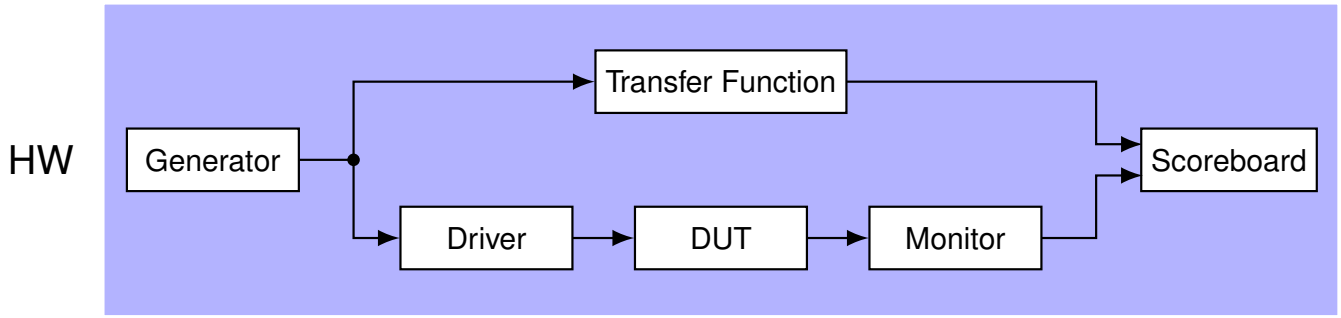


- HW Transfer Function

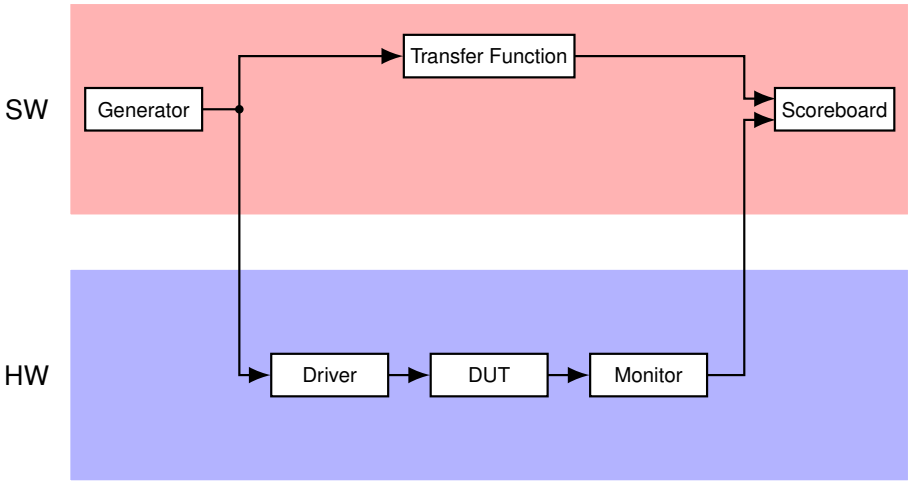
Experiments

- FrameLink protocol
  - FIFO
  - HGEN: hash generator (Bob Jenkins's *Lookup2*)
  - HGEN$\times k$

Component	Slices
FIFO	420
HGEN	947
HGEN$\times$2	2,152
HGEN$\times$4	3,762
HGEN$\times$8	7,448
HGEN$\times$16	15,778

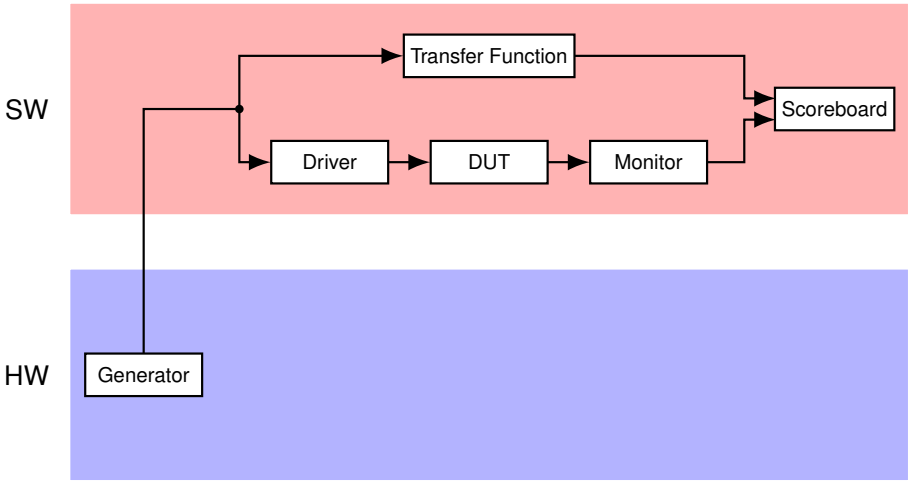
Results of Experiments

- HW-DUT



FIFO	3.062
HGEN	7.089
HGEN×2	23.458
HGEN×4	33.688
HGEN×8	52.896
HGEN×16	117.708

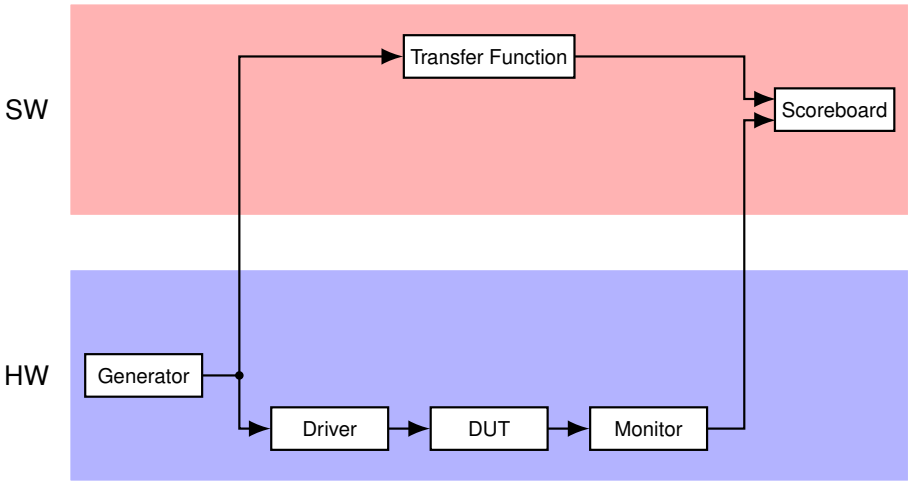
- HW-GEN



FIFO	0.743
HGEN	1.036
HGEN×2	1.023
HGEN×4	0.815
HGEN×8	0.776
HGEN×16	0.750

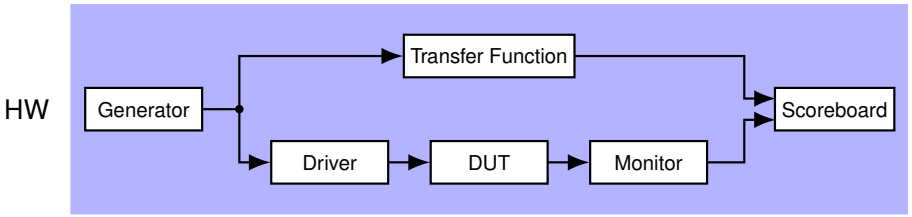
Results of Experiments

- HW-GEN-DUT



FIFO	2.689
HGEN	14.500
HGEN×2	93.833
HGEN×4	134.750
HGEN×8	195.308
HGEN×16	434.615

- HW-FULL



FIFO	13,429.0
HGEN	15,564.0
HGEN×2	54,925.0
HGEN×4	67,626.0
HGEN×8	74,347.0
HGEN×16	137,875.0

Conclusion

- 5 testbed architectures
- acceleration over 100,000$\times$
- free & open source

Future work

- automate synthesis
- reach coverage closure
- post-silicon verification